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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/846,119	04/30/2001	Yitzhak Gilboa	5298-04700 PM00028	5235

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CONLEY ROSE, P.C.
P.O. BOX 684908
AUSTIN, TX 78768

EXAMINER	
GOUDREAU, GEORGE A	

ART UNIT	PAPER NUMBER
1763	

DATE MAILED: 10/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/846,119	GILBOA ET AL.	
	Examiner	Art Unit	
	George A. Goudreau	1763	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16,19,22-27,29 and 30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16,19,22-27,29 and 30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. The finality of the last office action is withdrawn.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103© and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-16, 19, 22-27, and 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (6,063,689) further in view of Sethuraman et. al. (5,972,124). Chen et. al. disclose a process for forming an STI structure (124) on the surface of a wafer (100) which is comprised of the following steps:

-A bilayer mask (102, 104) is formed onto the surface of the Si wafer. Layer 102 is comprised of a pad SiO2 layer. Layer 104 is comprised of Si3N4. The bilayer mask is then patterned to form an etch mask.;

-The bilayer etch mask is then used in the etching of a trench in the Si wafer (100).;

-A SiO2 layer (116) is used to planarize the surface of the wafer as well as to fill the trench etched into the Si wafer.;

-The SiO2 layer (116) is then planarized, and etched using a two step process. During the first step, the SiO2 layer is cmp polished to planarize it. The planar SiO2 layer is then etched back in a plasma until the surface of the polysi layer (104) is reached which functions as a type of etch stop.; and

-The polysi, and SiO2 etch mask is then removed from the surface of the wafer using an etching process to leave behind an STI structure on the surface of the wafer.

This is discussed specifically in columns 3-4; and discussed in general in columns 1-6. This is shown in figures 1-2. Chen et. al. fail, however, to disclose the following aspects of applicant's claimed invention:

-the specific usage of a fixed abrasive pad, and a cmp slurry which contains no free floating abrasive particles to cmp polishing the surface of the SiO2 layer in the process taught above;

-the reduction of the thickness of the SiO2 fill layer to the specific thicknesses which are claimed by the applicant in the cmp polishing step;

-the specific formation of the etch mask layer used to form the trench in the Si wafer out of a SiO2 pad layer/ a Si3N4 pad layer; and

-the formation of the Si3N4 etch mask layer to the specific thicknesses which are claimed by the applicant

Sethuraman et. al. teach it is desirable to use a fixed abrasive cmp polishing pad in combination with a cmp slurry which contains no free floating abrasive particles when selectively cmp polishing a SiO2 layer to an underlying Si3N4 layer on a wafer in order to reduce the amount of over polishing of the Si3N4 polish stop which would be obtained as compared to a conventional cmp polishing process which employs an abrasive free polishing pad in combination with a cmp slurry which contains free floating abrasive particles. They further teach that it is desirable to use such a process since it avoids the costly necessity of disposing of

an abrasive cmp slurry. They further teach that it is desirable to use a SiO2 pad layer/ Si3N4 pad layer as an etch mask when forming STI trench in a CZ-Si wafer. This is discussed specifically in columns 1-2, 5-6, and discussed in general in columns 1-8. This is shown in figures 1-4.

It would have been obvious to one skilled in the art to conduct the cmp polishing process of Chen et. al. as taught above employing a fixed abrasive cmp polishing pad in combination with a cmp slurry which contains no free floating abrasive particles based upon the teaching of Sethuraman et. al. that it is desirable to do so for the same reasons as those stated above.

It would have been obvious to one skilled in the art to form the etch mask used in the etching of the STI trench in the Si wafer in the process taught above out of a combination of a SiO2 pad layer/ Si3N4 pad layer based upon the teachings of Sethuraman et. al. that it is desirable to do so. Further, this simply represents the usage of an alternative, and at least equivalent means for forming an etch mask in the process taught above to those means which are specifically taught above.

It would have been obvious to one skilled in the art to cmp polish the SiO2 layer in the process taught above until the thickness is reduced to the specific thicknesses which are claimed by the applicant base upon the following. It would have been obvious to one skilled in the art to use the cmp polish step to a sufficient extent to adequately, and rapidly planarize the surface of the SiO2 layer without undesirably exposing the surface of the underlying layer based upon the teachings in this reference regarding these matters.

It would have been obvious to one skilled in the art to form the Si3N4 etch mask in the process taught above to the specific thicknesses which are claimed by the applicant based upon the following. It would have been obvious to one skilled in the art to form adequate thickness to the Si3N4 layer in the process taught above such that an adequate level of protection is provided to the underlying layers during each etching step without forming an inordinately thick layer of

material which would adversely effect processing costs, and processing times for fabricating the device.

5. Claims 1-16, 19, 22-27, and 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (6,136,713) further in view of Sethuraman et. al. (5,972,124). Chen et. al. disclose a process for forming an STI structure (206 b) on the surface of a wafer (200) which is comprised of the following steps:

-A Si3N4 etch mask (202) is formed onto the surface of the Si wafer.;

-The Si3N4 etch mask is then used in the etching of a trench in the Si wafer (200).;

-A SiO2 layer (206) is used to planarize the surface of the wafer as well as to fill the trench etched into the Si wafer.; and

-The SiO2 layer (206) is then planarized, and etched using a two step process. During the first step, the SiO2 layer is cmp polished to planarize it. The planar SiO2 layer is then etched back in a plasma until the surface of the Si3N4 layer (202) is reached which functions as a type of etch stop.

This is discussed specifically in columns 3-4; and discussed in general in columns 1-6. This is shown in figures 1-2. Chen et. al. fail, however, to disclose the following aspects of applicant's claimed invention:

-the specific usage of a fixed abrasive pad, and a cmp slurry which contains no free floating abrasive particles to cmp polishing the surface of the SiO2 layer in the process taught above;

-the reduction of the thickness of the SiO2 fill layer to the specific thicknesses which are claimed by the applicant in the cmp polishing step;

-the formation of the Si3N4 etch mask layer to the specific thicknesses which are claimed by the applicant; and

-the specific formation of the etch mask layer used to form the trench in the Si wafer out of a SiO2 pad layer/ a Si3N4 pad layer

It would have been obvious to one skilled in the art to conduct the cmp polishing process of Chen et. al. as taught above employing a fixed abrasive cmp polishing pad in combination with a cmp slurry which contains no free floating abrasive particles based upon the teaching of Sethuraman et. al. that it is desirable to do so for the same reasons as those stated above.

It would have been obvious to one skilled in the art to form the etch mask used in the etching of the STI trench in the Si wafer in the process taught above out of a combination of a SiO2 pad layer/ Si3N4 pad layer based upon the teachings of Sethuraman et. al. that it is desirable to do so. Further, this simply represents the usage of an alternative, and at least equivalent means for forming an etch mask in the process taught above to those means which are specifically taught above.

It would have been obvious to one skilled in the art to cmp polish the SiO2 layer in the process taught above until the thickness is reduced to the specific thicknesses which are claimed by the applicant base upon the following. It would have been obvious to one skilled in the art to use the cmp polish step to a sufficient extent to adequately, and rapidly planarize the surface of the SiO2 layer without undesirably exposing the surface of the underlying layer based upon the teachings in this reference regarding these matters.

It would have been obvious to one skilled in the art to form the Si3N4 etch mask in the process taught above to the specific thicknesses which are claimed by the applicant based upon the following. It would have been obvious to one skilled in the art to form adequate thickness to the Si3N4 layer in the process taught above such that an adequate level of protection is provided to the underlying layers during each etching step without forming an inordinately thick layer of material which would adversely effect processing costs, and processing times for fabricating the device.

6. Applicant's arguments with respect to claims of record have been considered but are moot in view of the new ground(s) of rejection.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner George A. Goudreau whose telephone number currently is (703) -308-1915. My telephone number will be changing to (571)-272-1434 at some time during December 2003 due to my relocation to the new patent office facility. The examiner can normally be reached on Monday through Friday from 9:30 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Examiner Gregory Mills, can be reached on (703) -308-1633. The appropriate fax phone number for the organization where this application or proceeding is assigned currently is (703) -306-3186. My fax number will be changing to (571)-273-1434 at some time during December 2003 due to my relocation to the new patent office facility.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) -308-0661.

George A. Goudreau/gag
Primary Examiner
AU 1763